REMARKS

The Office Action mailed June 1, 2004 has been received and the Examiner's comments carefully reviewed. Claim 1 has been amended as supported by, for example, Figures 1 and 2 of the present specification. No new matter has been added. Favorable reconsideration of this application is requested in view of the following remarks.

Claim Rejections - 35 USC § 102

In the Office Action, claim 1 has been rejected as anticipated by JP 2000173802; claims 1 and 2 have been rejected as anticipated by Yoneda; claim 1 has been rejected as anticipated by Tsukada; claims 1-3 have been rejected as anticipated by Nakanishi et al. Applicants respectfully traverse these rejections.

Claim 1 recites, among other things, a chip resistor comprising an outermost cover coat having an outermost surface and an auxiliary upper electrode including an outer edge and an inner edge, the inner edge held in direct contact with the outermost surface of the outermost cover coat, wherein said outer edge of the auxiliary upper electrode projects beyond the outermost surface of the outermost cover coat, the auxiliary upper electrode having a thickness that decreases progressively from said outer edge to said inner edge such that the thickness of the auxiliary upper electrode is maximum at said outer edge and minimum at said inner edge. None of the JP 2000173802, the Yoneda, the Tsukada, or the Nakanishi et al. references, either alone or in a reasonable combination with others, discloses or suggests a chip resistor with the features specified in claim 1.

In the chip resistor disclosed by JP 2000173802, the outer edges of the auxiliary upper electrodes 12, 13 do not project beyond the outermost surface of the cover coat 7. The inner edges 12a, 13a, instead, project beyond the outermost surface of the cover coat. Such a structure fails to provide a stable support for the chip resistor because the distance between the two mounting points (in this configuration, the distance between the inner edges 12a, 13a) is not maximized and is relatively short. Furthermore, the thickest part of the auxiliary upper electrode of the JP 2000173802 reference is shown to be at the inclined intermediate portion of the electrode, rather than at the outer edge of the electrode, as required by claim 1.

In the chip resistor disclosed by Yoneda, three protective films or coats (51, 52, and 53) are formed on the resistor film. The outermost surface of the outermost cover coat in Yoneda corresponds to the upper surface of protective film 53. The entirety of auxiliary upper electrodes 24, 34 is located below the outermost surface of the cover coat 53 and the outer edges of the auxiliary electrodes do not project beyond the outermost surface of the cover coat, as required by claim 1. A chip resistor with a configuration such as the one in Yoneda cannot be mounted in a reverse posture, which is an advantage provided by the present invention.

In the chip resistor disclosed by Figure 17 of Tsukada, although the outer edges of the auxiliary upper electrodes 28 project beyond the outermost surface of the overcoat layer 29, the thickness of each auxiliary electrode does not decrease progressively from the outer edge to the inner edge such that the thickness is maximum at the outer edge and minimum at the inner edge, as required by claim 1. The auxiliary upper electrode disclosed in Figure 17 has its maximum thickness at its intermediate portion.

Lastly, in the chip resistor disclosed by Nakanishi et al., the outermost surface of the outermost cover coat corresponds to the upper surface of protective layer 29. The entirety of the upper electrodes 25 is located below the outermost surface of the protective layer 29, as in the Yoneda reference, and the outer edges of the auxiliary electrodes do not project beyond the outermost surface of the cover coat, as required by claim 1.

For at least these foregoing reasons, claim 1 is patentable over JP 2000173802, Yoneda, Tsukada, and Nakanishi et al.

Claims 2 and 3 depend from claim 1 and are believed to be patentable over Yoneda and Nakanishi et al. for at least the same reasons specified with respect to claim 1.

Favorable reconsideration of the claims in the form of a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference would advance the prosecution of this application, the Examiner is invited to telephone the undersigned at the below-listed telephone number.

Respectfully submitted,

MERCHANT & GOULD P.C.
P.O. Box 2903
Minneapolis, Minnesota 55402-0903
(612) 332-5300

Date: August 27, 2004

Douglas P. Mueller
Reg. No. 30,300
DPM/AS/jt